

ECS 409/609 : Verilog/VHDL

Structural (Gate Level) Based Assignment

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Structural (Gate-Level) Module

- This module of the Verilog contains gate level description of the circuit.
- Describe how modules are connected.
- Each module contains the instances of other modules and the interconnection between them.

Sample Structure of Structural (Gate-level) Verilog Coding Style

As shown in Figure 1, the `top` module is built from the instance of two module `small`. The structural code of the `small` module is as follows:

```
module small (A, B, Y);  
input A;  
input B;  
output Y;  
// description of module small  
endmodule
```

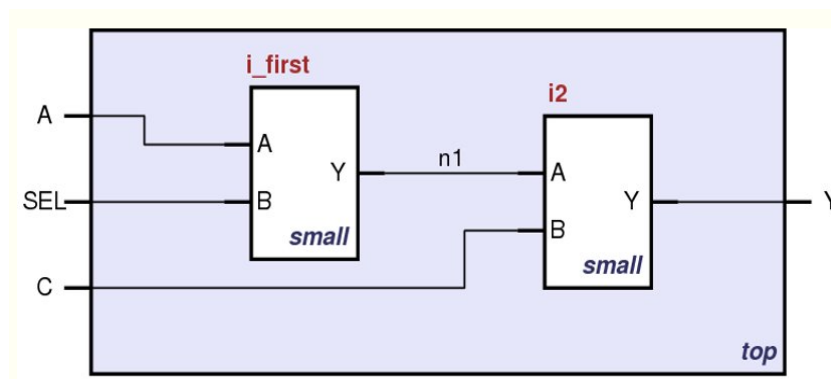


Figure 1: Structural Schematic Module

Whereas, the structural code of the `top` module are as follows:

```
module top (A, SEL, C, Y);
input A, SEL, C;
output Y;
wire n1;

// instantiate small once
small i_first ( .A(A), .B(SEL), .Y(n1));

//instantiate small second time
small i_second ( .A(n1), .B(C), .Y(Y));

endmodule
```

With this module in mind, implement the following Verilog programs using Structure (Gate-Level) Verilog.

Problem Statements

Level-Easy

Problem 1: Implement a structural Verilog model for a 3-input AND gate, 3-input OR gate.

Problem 2: Implement a structural Verilog model for a 4-bit magnitude comparator.

Level-Medium

Problem 3: Develop a structural Verilog model for a half adder and subtractor using basic gates and a full adder/subtractor using basic gates.

Problem 4: Implement a structural Verilog model for a 4-to-1 multiplexer and 3-to-8 decoder.

Level-Difficult

Problem 5: Create a structural Verilog model for a 4-bit barrel shifter with (1-bit and 2-bit) left and right shift.

Problem 6: Create a structural Verilog model for a simple-bit ALU that supports addition, subtraction, multiplication, logical AND, logical OR, and logical XOR. Use Op-Code to specify the operation.