Computer Organization Lab (ECS 409/609)

IISER

Mid-semester Examination (5 Questions, 30 Max Points) **Bhopal, India**

Time: 3:00–4:00 pm (60 minutes) Pages: 2 **28 Sept. 2024 (Sat.)**

INSTRUCTIONS

1. **Write name and RollNo in the space provided below and also on the answer book(s).**
2. **Printed, photocopied, phone, calculator etc. and exchange of any material is NOT allowed.**
3. **At the end of examination, return the question paper and answer book(s).**
4. **Solve questions serially in the answer script.**

RollNo | | | | | | | | | | **Name:**

Question	1	2	3	4	5	Total
Points	2	3	5	10	10	30
Score						

1. (a) Write the behavioral statement for 3-input `NAND` gate using `AND` and `NOT` operator and assign it to output `y`. The gate has a delay of 2 time units. [2]

2. (a) We have declared two sets of wires as follows: [3]

```
wire [2:0] w1, w2;
wire [5:0] bundle;
```

Write a Verilog statement to create the `bundle` using most significant bit of `w1` and least significant bit of `w2`.

3. (a) Does the following verilog code result in a sequential circuit or combinational circuit? Reason your answer as well. [5]

```
module IdentifyCKT(input [1:0] in_data, input mask, output reg [1:0] out_data);
always @ (*)
 begin
  out_data[1] = in_data[1];
  if (mask)
    out_data[0] = 0;
  end
endmodule
```

4. (a) Implement the behavioral verilog module called `PrimeAndDiv` in your simulator. The `PrimeAndDiv` module receives four inputs $A_{3:0}$, and two outputs, `P` and `D`. The input $A_{3:0}$ represent a number from 0 to 15. Output `P` should be `True`, if the number is prime [10]

(note that 0 and 1 are not prime, but, 2, 3, 4 and so on, are prime). Output `D` should be `TRUE` if the number is divisible by 3.

5. (a) Implement the structural Verilog module to compute the logic function `F(A, B, C)` in your simulator. 10

`F(A, B, C) =` A$\bar{B}$ + $\bar{B}\bar{C}$ + $\bar{A}$BC