Computer Organization Theory (ECS 409/609)

IISER

Mid-semester Examination (5 Questions, 30 Max Points) **Bhopal, India**

Time: 4:00–5:30 pm (90 minutes) Pages: 2 **28 Sept. 2024 (Sat)**

INSTRUCTIONS

1. **Printed, photocopied, phone, calculator etc. and exchange of any material is NOT allowed.**
2. **Solve questions serially in the answer script.**

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1. (a) Consider the 32 bit Hexadecimal number `0xcafe2b3a`. [2]
   1. What is the binary representation of a number in little-endian format? Mark the bytes and number them from low (0) to high (3) bytes.
   2. What is the binary representation of a number in big-endian format? Mark the bytes and number them from low (0) to high (3) bytes.

   (b) Suppose `32-bit` instruction using the following format: [2]
   If there are 250 opcodes and 125 registers

Opcode	DR	SR1	SR2	Unused

   1. Determine the minimum number of bits required to represent the opcode.
   2. What is the minimum number of bits required to represent the Source register `(SR1 or SR2)`.
   3. What is the minimum number of bits Unused in the instruction encoding?

   (c) 1. Compute $3 - 5$ using 4-bit two's complement numbers. [2]
   2. Define a combinational circuit.

2. (a) Design an ALU that takes as input two N bit strings A, B and outputs the result of the following operation according to the value of additional input F. Please highlight how values of F affect the circuit. For smaller circuits like AND, OR, ADDITION you can use their schematic presentation. [4]

F	0	1	2	3	4	5	6	7
Operation	A AND B	A OR B	A + B	not used	A AND $\overline{B}$	A OR $\overline{B}$	A - B	SLT

   (b) What is the delay for (i) a ripple-carry adder and (ii) a carry-lookahead adder with 4-bit blocks of 64-bit adders? Assume that each two-input gate delay is 150 ps and that a full adder delay is 450 ps. [2]

3. (a) Define a finite state machine and draw state diagram for the danger sign controller. Assume that the danger sign has five LEDs making an arrow sign that suggests to 'move right'. [2]

   (b) Design a sequential logic circuit for the danger sign controller and draw its outline using two CLUs and two storage elements. [1]

   (c) Draw gate-level description of the two CLUs used. [3]

4. Simplify the following Boolean equations using Boolean theorems. Show your steps and verify it using K-maps.

   (a) $Y = AC + \bar{A}\bar{B}C$ [1]

(b) $Y = \bar{A}\bar{B} + \bar{A}C\bar{B} + (A \bar{+} \bar{C})$ 2

(c) $Y = \bar{A}\bar{B}\bar{C}\bar{D} + A\bar{B}\bar{C} + A\bar{B}C\bar{D} + ABD + \bar{A}\bar{B}C\bar{D} + B\bar{C}D + \bar{A}$ 3

5. (a) Given the data path of LC-3 in Figure 1, with a semantic of Store `ADD` instruction as outlined below, list the correct sequence of every control signal set by the FSM to implement the instruction processing cycle. The instruction processing cycle includes Fetch, Decode, Evaluate Address, Fetch Operand, Execute, and Store Results. 6

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ADD R0, R1, R2                    // R0=R1+R2
```

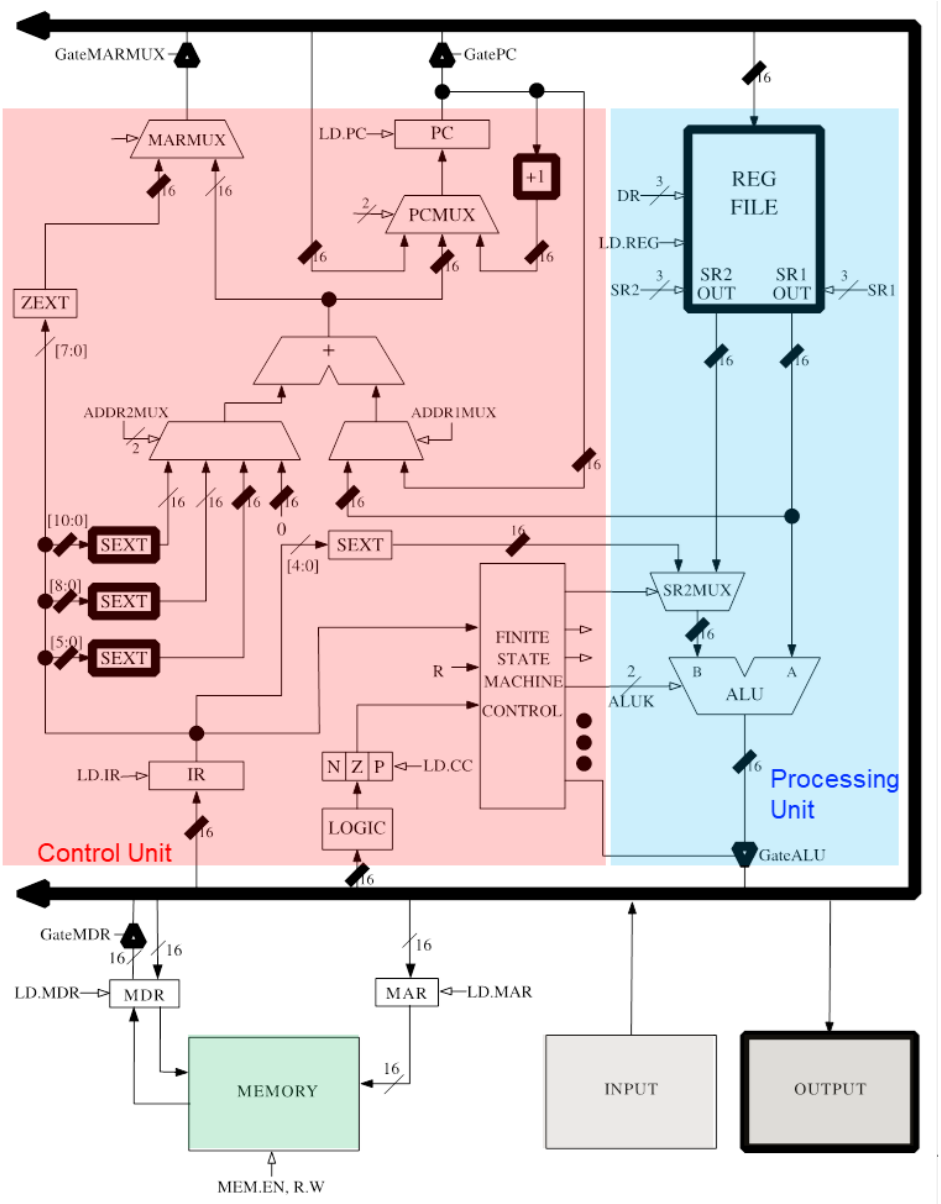

Figure 1: ISA Section Figure