ECS 409/609 Computer Organization: Quiz-01 (for 30 pts)

1. (a) (4 pts) Identify which of the following combinational logic blocks does the following verilog code implement? Justify your answer.

```
module mystery(d0, d1, d2, d3, d4, d5, d6, d7, a, b, c);
    input d0, d1, d2, d3, d4, d5, d6, d7;
    output a, b, c;
    or(a, d4, d5, d6, d7);
    or(b, d2, d3, d6, d7);
    or(c, d1, d3, d5, d7);
endmodule
```

   A. 3:8 Decoder (3:8 means 3 input and 8 output)
   B. 8:1 Multiplexer
   C. 8:3 Priority Encoder
   D. None of the above

   (b) (2 pts) Using five bits to represents each number, write the representation of 7 and -7 in signed magnitude and 2's complement.

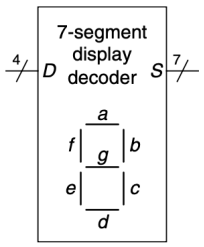
2. (a) (4 pts) Identify the mistake(s) (if any) in the following Verilog code that implements 4:1 multiplexer.

```
module mux4(input  [3:0] d0, d1, d2, d3
            input [1:0] s,
            output [3:0] y);
            assign y = (s == 2'b11) ? d2 :
            (s == 2'b10) ? d3 :
            (s == 2'b01) ? d0 :
            d1;
  endmodule
```

   (b) (2 pts) Briefly describe the seven levels of transformation discussed in the class.

3. (a) (2 pts) Draw gate-level description of a a $3:8$ decoder.

   (b) (4 pts) Consider a seven-segment display decoder in the figure. Suppose S_b denotes the output corresponds to segment b. Write a truth table for S_b and derive a (compact) boolean equation for the same using K-maps. Illustrate your steps.



4. (a) (2 pts) Define sequential logic circuits and describe flip-flop switch.

   (b) (4 pts) Draw truth table and gate-level description of a full one-bit adder.

5. (3pts + 3pts) Describe Carry-Lookahead Adder (CLA) using boolean equations. Make these equations explicit for the 4-bit adder. Finally, draw a digital logic circuit for the 4-bit adder.