Computer Organization Theory (ECS 409/609)

IISER

Quiz-2 (4 Questions, 30 Max Points) — **Bhopal, India**

Time: noon – 1 pm (60 minutes) Pages: 2 — **9th Nov 2024 (Sat)**

INSTRUCTIONS

1. **Printed, photocopied, phone, calculator etc. and exchange of any material is NOT allowed.**
2. **Solve questions serially in the answer script.**

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1. (a) A memory addressability is 16 bits. What does that say about the size of MAR and MDR? [2]

   (b) Consider a 16-bit LC-3 processor (i.e., each instruction is 16-bit wide). A typical LC-3 instruction looks like *ADD, Destination, Source, and Immediate*, where destination and source are the registers and immediate is the 5-bit immediate value. The first 4-bits of the instruction are used to distinguish the opcode. [6]

   1. Determine the maximum number of registers that a processor can support.
   2. Radhe wishes to execute a single LC-3 instruction to subtract the decimal 21 from the Source register and store the result back to the Destination register. If this is the case, can Radhe perform the subtraction? If yes, show how it would be done. If no, describe the reason.

2. (a) For the given assembly program. Note that PC^* is incremented PC. [4]

Address	**Semantics**
0x4222	$R3 \leftarrow PC^* - 4$
0x4223	$R4 \leftarrow R3 + 11$
0x4224	$R9 \leftarrow R9$ & 0
0x4225	$Mem[PC^* - 7] \leftarrow R4$
0x4226	$R2 \leftarrow R9 + 13$
0x4227	$Mem[R3 + 11] \leftarrow R2$
0x4228	$R1 \leftarrow Mem[Mem[PC^* - 10]]$

   1. Identify the addressing mode used at every address.
   2. Determine the final value of R1.

   (b) The condition codes have values `N = 0`, `Z = 1`, and `P = 0` at the beginning of the execution of the following sequence of LC-3 instructions. Note that `R0` contains a large positive number. [4]

```
AND R0, R0, #0
ADD R0, R0, #2
NOT R1, R0
ADD R1, R1, #31
AND R2, R0, R1
ADD R3, R2, #32
```

   Determine the value of condition codes at each instruction when the following program is executed.

3. (a) A program executes 600 billion instructions. It runs on an Intel processor with an average CPI of 0.8 and a clock frequency of 3.2 GHz. [4]

- How many seconds does the program take to execute?
- What is the cycle time of the Intel processor?
- Assume that an AMD processor takes 100 seconds to finish the program. What is the speed-up provided by the AMD processor relative to the Intel processor?

(b) Consider a 4-stage pipeline with a delay of 20, 40, 60 and 90 nano second. With this information, calculate the following: [4]

1. Pipeline Cycle time
2. Non-pipeline execution time
3. Speedup by Pipeline over Non Pipeline machine
4. Pipeline time for 1000 instructions
5. Non pipeline time for 1000 instructions
6. Pipeline Throughput (number of instructions executed per unit time)

4. (a) Write machine instruction format for for `lw` instructions and explain every term in it. [2]

(b) Consider the state elements of MIPS processor shown in Figure 1. Using these, design a datapath for single cycle processor for `lw` instructions. Write every connection point-wise. Suppose the instruction memory fetches instruction labeled *Instr*. Show control signals wherever necessary. [4]

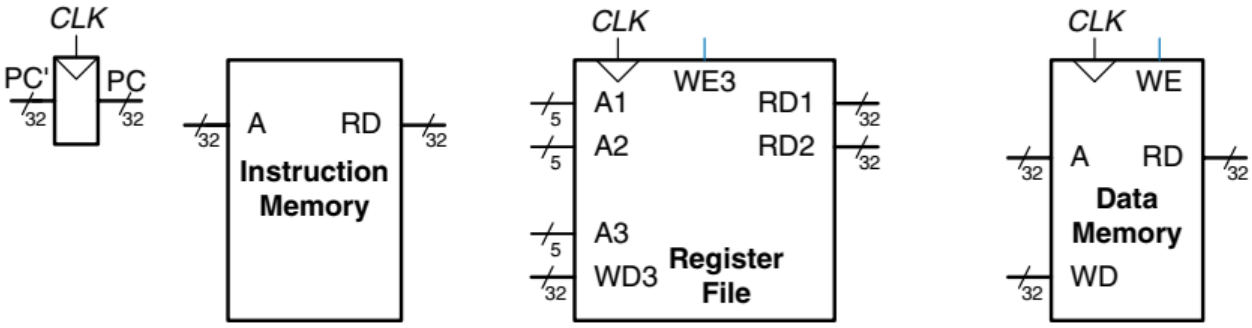

Figure 1: State elements of MIPS processor